PlatformConference

Direction • Design • Perspective • Analysis

A Trend to Future Platform and Chipset Integration - Wireless & High Speed Links Technologies

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Chipset I/O Trends

- Chipset Southbridge define I/O of the system
  - Integration of I/O functions depends on market demand
- I/O moves from Parallel to high speed Serial to save pins, cost and alleviate ease-of-use
  - PCI -> HyperTransport™, 3GIO
  - SIO -> USB, IEEE 1394
  - ATA -> Serial ATA
- High-speed Wireless Interface Technology
  - 802.11, Bluetooth™ just another form of I/O
- PHY (RF) integration and partitioning
  - Cost, performance and stability trade off
  - Industry-standard Link-PHY (RF) interface

Agenda

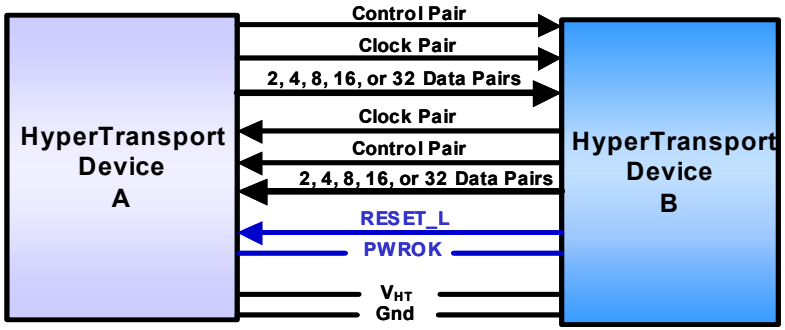
- High-speed Wired Interface Technology
  - HyperTransport™
  - 3GIO
  - Serial ATA
  - USB
  - IEEE 1394
- High-speed Wireless Interface Technology
  - 802.11
  - Bluetooth™
  - Concern & Resolution

HyperTransport™

- Efficient chip-to-chip Interconnect
  - QoS & isochrony
    - Low latency with no data-encoding
    - Coherency option facilitates processor-to-processor communications
  - Scaleable bandwidth
    - By frequency (increment of 200MHz)
    - By bus-width of 2-, 4-, 8-, 16-, or 32-bit wide in each direction
  - Simpler I/Os
    - Differential
    - No clock recovery
  - Power-friendly
    - Each link can be configured to run at a multiple of 200MHz, up to max. 800MHz.

HyperTransport™ Basics

- A HT-bus has two uni-directional point-to-point Links
  - Each Link can be 2-, 4-, 8-, 16-, or 32-bit wide in each direction
- @ 800MHz clock, up to 3.2GB/s for 8-bit each-way Links
  - 24x the bandwidth of PCI-32/33 with less pins (55 vs. 84)
- Packets are multiple of 4-Bytes in length
- Serial link with commands, data and addresses use the same bits
- Signal to GND ratio ~ 4:1
- Optional Link power-down signals for mobile
  - HyperTransportDeviceStop_L, DevReq_L
  - Power per pin-pair is '0' when in HyperTransportDeviceStop mode
- PCI compatible



PWROK, RESET_L required for proper reset & initialization
V_{HT} routed between devices for proper common mode range

Bus Width (Each Way)	2	4	8	16	32
Data Pins (total)	8	16	32	64	128
Clock Pins (total)	4	4	4	8	16
Control Pins (total)	4	4	4	4	4
Subtotal (high speed)	**16**	**24**	**40**	**76**	**148**
VLDT	2	2	3	6	10
GND	4	6	10	19	37
PWROK	1	1	1	1	1
RESET_L	1	1	1	1	1
Total Pins	**24**	**34**	**55**	**103**	**197**
Total Max BW GB/s	**0.8**	**1.6**	**3.2**	**6.4**	**12.8**

DC Power per Pin-Pair: 4 ~ 9 mW, 6 $mW_{Typical}$
Signal to V_{HT}/Gnd Ratio: 4:1

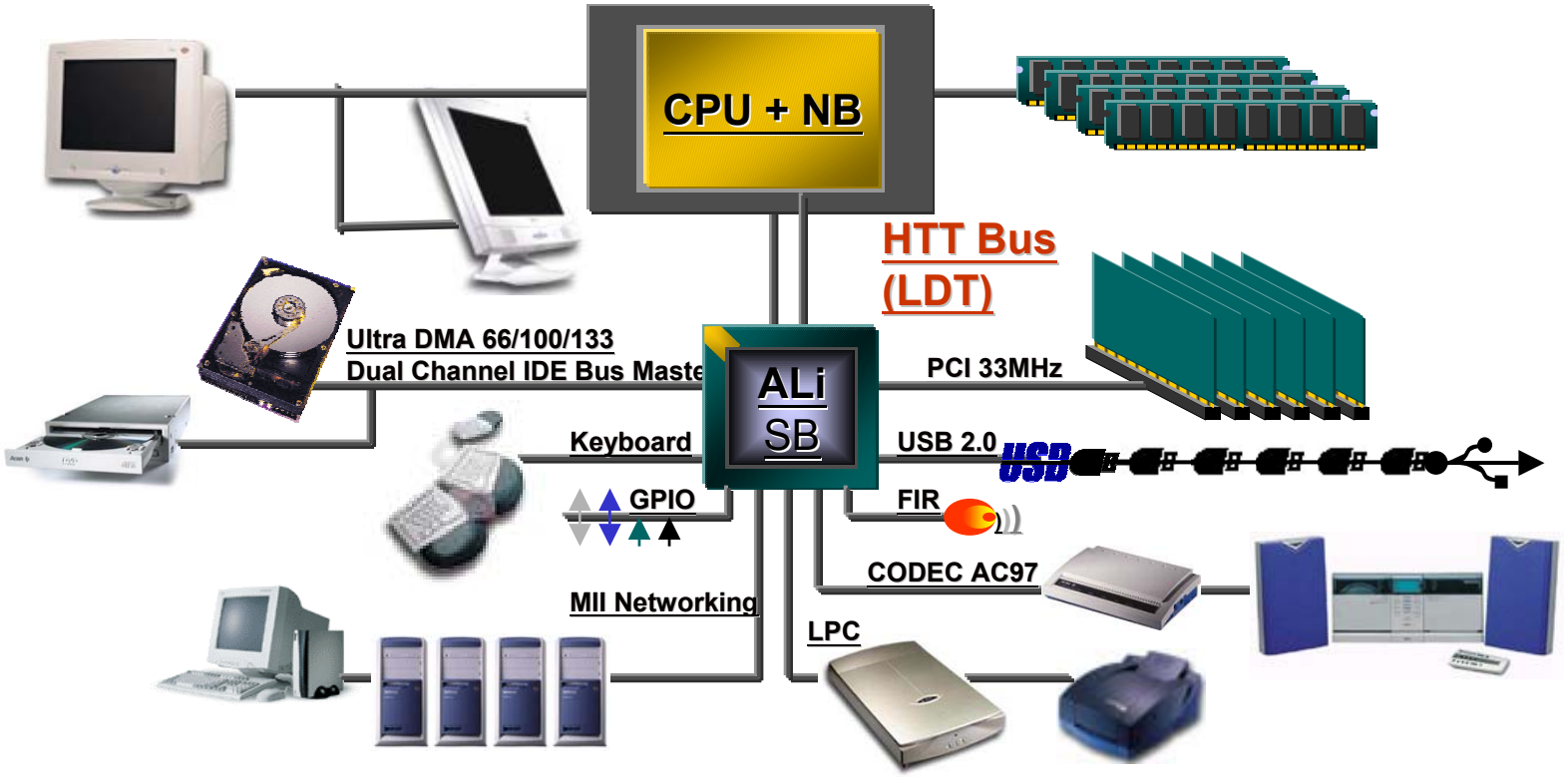
HyperTransport™ Adoption

- CY2001
  - PC core logics chipsets since Q3CY01
  - Network processors from Broadcom & PMC-Sierra in Q4CY01
  - Key component of proposal for LA2 Look-at-Side I/F at Network Processor Forum
  - FPGA products from Altera
- Future
  - More PC core logics chipsets to be released
  - Applications across computing, embedded, CE segments
    - x86-, MIPS-based processors with integrated HT-bus
    - Network processors to be released: Sandcraft, ...
  - Magamacro from IP providers and design houses

HTT PHY integration

- Industrial first open standard for chip-to-chip, high-speed low-latency serial interconnect
- No Link-PHY interface ever defined
- Integration already proven in volume shipment

ALi commitment to HTT



ALi HTT SB Key Attributes

- HyperTransport™ Technology (HTT)
  - Lightning Data Transport (LDT)
  - 8-bit LDT Links in each direction
  - At least 400 x 2 MB/s data transfer rate
- PCI Spec. v2.2 compliant
  - PCI 33MHz slots (support up to 6 REQ/GNT pairs)
- Enhanced DMA Controllers, Interrupt Controller, Counters / Timers
- ACPI v2.0 Power Management support
- Integrated IDE Controller for ATA 33/66/100/133
- USB Host Controllers with 6 ports to support USB Spec. 1.1 & 2.0

ALi HTT SB Key Attributes Cont.

- AC97 v2.2 Controllers for external audio and telephony codecs
  - Supports up to 6 channels and SPDIF In/Out
- Integrated 10/100 Mb/s Fast Ethernet MAC
- Low Pin Count (LPC) Interface for legacy function
- Integrated PS2/AT Keyboard controller and PS2 Mouse Controller
- Integrated 256-Byte SRAM Real-Time-Clock
- Integrated Fast Infrared Controller
- Integrated Memory Stick & Secure Digital Host Controllers

USB

- Bus-based interconnect for predominantly computing peripherals
- Mix of differential and single-ended signalings with data rates of 1.5Mb/s, 12Mb/s, 480Mb/s
- Master-slave packet-oriented protocol that support both asynchronous and isochronous transaction
- Hot add/remove electrical support with power distributed over the cable
  - Convenient for *light-weight* devices without power brick
- Versions 1.1 and 2.0 Hosts & Devices are compatible operationally
  - Won't hang each other

USB Adoption

- USB version 1.0 (1.5 & 12Mb/s) is in every PC shipped
- USB version 2.0 (480Mb/s) integrated PC core logics will be deployed in volume in H2CY02
  - Lack of standard digital interface between the PHY-equivalent and the Host-logics means high-speed mixed-signal integration and volume production simultaneously
- USB version 2.0 integrated peripherals in volume production since Q4CY01
  - Mass Storage first out-of-gate: CD-RW, hard disk drives
  - Scanner the next: Benq, UMAX, HP, Canon, Lexmark, …
  - PC desktop cameras & digital still-picture cameras the next

USB 2.0 PHY integration

- UTMI is tailored only for single-port peripheral type applications
  - No cost-effective interface defined for Host Controller implementation
  - Host Controller such as NEC move straight to PHY integration
- Almost all USB2.0-compliant Function Controllers by-pass UTMI, with the PHY fully integrated
  - 480Mb/s I/Os prove to be manageable by the industry at large
- Integration proven

IEEE 1394

- Bus-based interconnect predominantly for digital consumer electronics products
  - Effort undergoing to finalize IDB-1394 as the multimedia network for automotive applications
- Differential signaling with data rates of 100, 200, 400, 800, 1600, 3200Mb/s
- Peer-to-peer packet-based protocol that support asynchronous, isochronous and IP transactions
- Hot add/remove electrical support with power distributed over the cable
  - Convenient for *heavy-weight* devices without power brick
- Support transmission media of copper, glass & plastic optical fiber, wireless

IEEE 1394 PHY integration

- IEEE 1394 defines Link-PHY interface in Annex J
- Early implementation are multi-chip solution with Annex J Link-PHY interface
- Currently, most shipment are of single-chip implementation

Serial ATA

- Point-to-point serial interconnect for internal storage devices
- AC-coupled differential low-voltage signaling with clock embedded using 8B10B coding and data characters scrambled
- 1.5Gbps for 1st generation, and 3Gbps for 2nd generation
- Optional power management support
- Transparent to existing Win32 driver models

Serial ATA Adoption

- Product demonstration
  - PCI-based Serial ATA Host Controller
    - From Silicon Image in H1'01
    - From Adaptec & Promise at Comdex '01
  - Serial ATA hard disk drives
    - From Seagate in CY01
    - From Samsung, Fujitsu, Maxtor, Western Digital at Comdex '01
  - Parallel ATA (UDMA100) to Serial ATA Bridge IC from Marvell Semi at Comdex '01
- Integration of PHY into PC core logics is challenging & process dependent

Serial ATA PHY integration

- First generation Disk Controller uses separate PHY or Link-PHY with the Controller
  - Expect PHY integration to bring down cost but not proven yet
- Link-PHY industrial standard interface
  - On-going ad-hoc discussion, but no schedule in sight

3GIO

- Efficient point-to-point interconnect for *Slots*
  - AC-coupled differential low-voltage signaling with clock (1.25GHz) embedded using 8B10B coding
  - 2.5Gb/s per pair of Tx & Rx
    - @ 1.25GHz, up to 4GB/s for 8-bit each-way Link
      - 30x the bandwidth of PCI-32/33 with less pins (40 vs. 84)
  - Packet-based split-transaction protocol
  - Error management
  - Hot add/remove electrical support
    - Support connectors and cables for in-system and off-system applications
  - PCI configuration and driver model software compatible
  - Specification still in development
  - Co-existence with HTT

3GIO PHY integration

- No Link-PHY interface defined
- Interesting to see SATA PHY integration experience
  - Twice the I/O frequency of SATA

WLAN – 802.11

- Predominantly for wireless LAN in commercial and home environment
  - "Best effort" datagram service with CSMA/CA
  - Power management, roaming, security, QoS
- 3 major PHY specification that care share one single MAC implementation

	802.11a	802.11g	802.11b
Standard approved	9/1999	CY2002?	9/1999
Available Bandwidth	300MHz	83.5MHz	83.5MHz
Frequency of Operation	5.15 ~ 5.35GHz	2.4 ~ 2.4835GHz	2.4 ~ 2.4835GHz
Number of non-overlapping Channels	12	3	3
Data Rate per Channel	6, 9, 12, 18, 24, 36, 48, 54Mb/s	1, 2, 5.5, 11, 22Mb/s	1, 2, 5.5, 11Mb/s
Power Parameters in US	Tx: 23dBm @ gain 6dBi Rx sens.: -82 ~ -65dBm	TBD	Tx: 30dBm Rx sensitivity: -76dBm
Modulation Types	OFDM	DSSS (optional CCK-OFDM, PBCC	DSSS

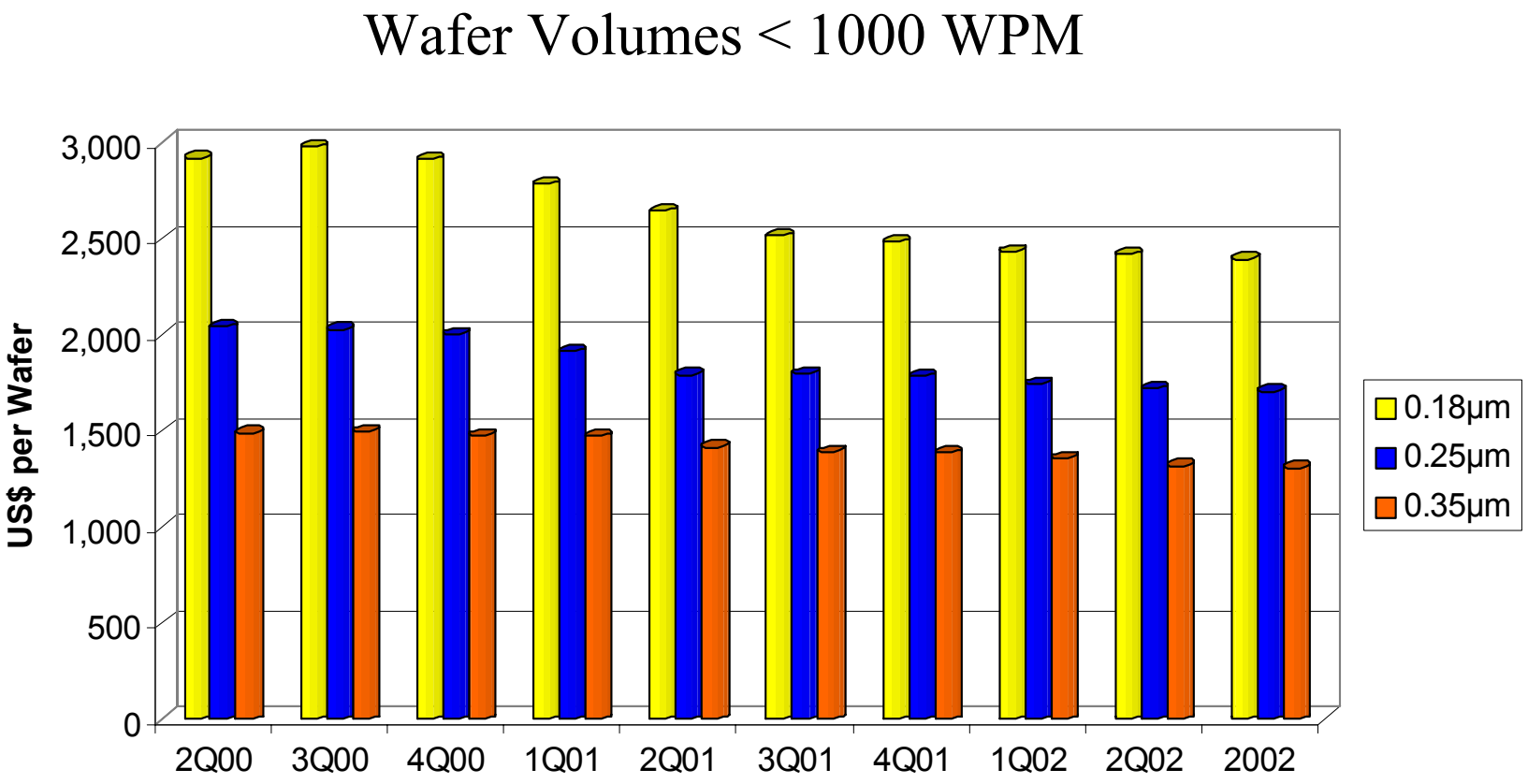
IEEE 802.11 Task Groups

- 802.11e for quality of service (QoS)
  - Enhance 802.11 MAC to improve and manage QoS to provide classes of service (e.g. video, audio, voice, data, …)
- 802.11f for multi-vendor AP interoperability
  - Develop recommended practices for Inter-Access Point Protocol (IAPP) to achieve distribution system wide multi-vendor access point interoperability
- 802.11g for higher-rate 802.11b
  - Develop new PHY extension to enhance the performance of 802.11b-compatible networks by increasing the achievable data rate
- 802.11i for advanced security
  - Enhance the 802.11 MAC to improve security and authentication mechanisms
- 802.11h for regulatory approval in Europe
  - Enhance the 802.11 MAC and 802.11a PHY to provide Dynamic Frequency Selection (DFS) and Transmit Power Control (TPC)
- Most Task Groups should be conclude by Q4CY02

Bluetooth™

- Predominantly for Wireless Personal Area Network (WPAN)
  - Master connects up to 7 simultaneous or 200+ active slaves per piconet
  - Scatternet forms by up to 10 piconets within range
- Data rate of 1MS/s (720Kb/s) for version 1.1
  - 10 meters or less, up to 100 meters with PA
- Operates in unlicensed ISM 2.4GHz
  - Frequency hopping with GFSK modulation
  - Packetized protocol with TDMA/TDD (time-division duplexing) to support isochrony
    - 79 channels of 1MHz wide each
- Power Friendly
  - Low transmit power with no equalization for multipath
  - Low-power modes: *park*, *sniff*, *standby*
  - Power reduction at system, algorithm, logic, and circuit abstraction

The Cost of CMOS Wafers….Not all are the same.



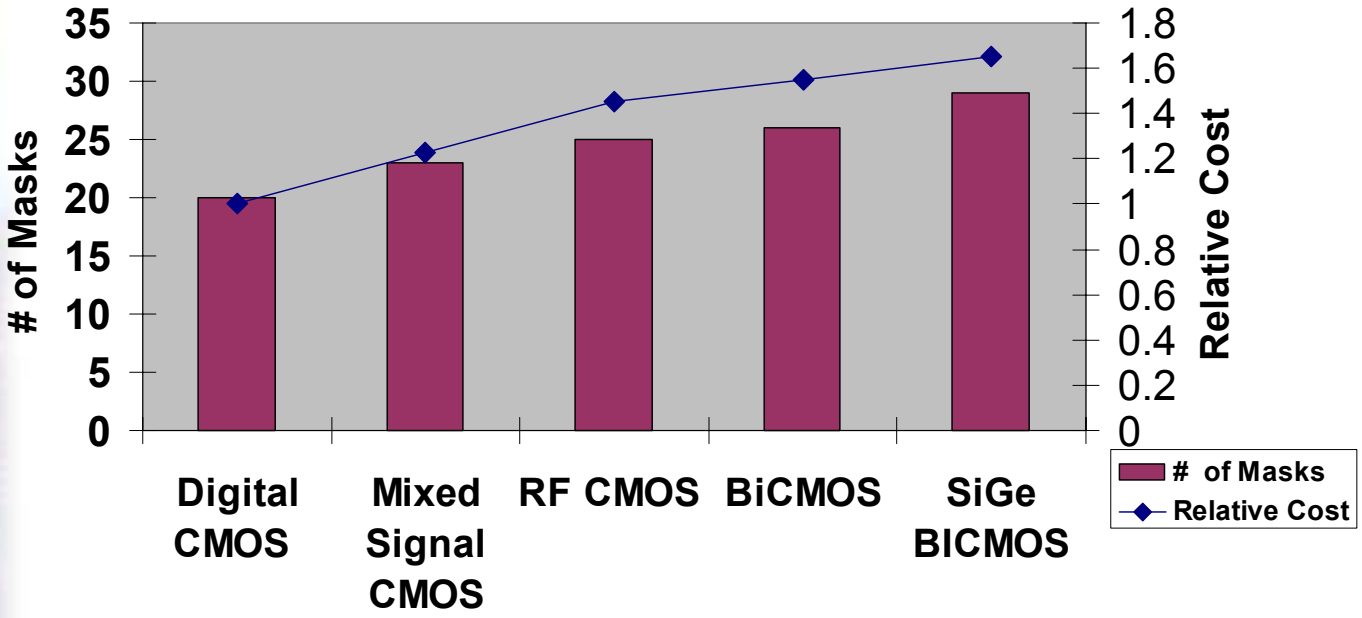
Average Wafer Cost vs Device Feature Size (CMOS Gate Length)

Source: Semico Research Corp.

Cost Impact of Technology Selection

- Digital CMOS
  - Base process in most (all) commercial radio and baseband IC product implementations
- CMOS Radio Implementation
  - Good RF performance requires additional process steps in manufacturing (RF CMOS)
    - Thick Metal (Inductors)
    - RF Capacitors (MIM, MOM)
    - Linear (analog) Resistors
    - Dual Voltage CMOS
- BiCMOS (or SiGe BiCMOS) Radio Implementations
  - A few more steps……Is the cost significant?

Relative Cost/Complexity of Si Semiconductor



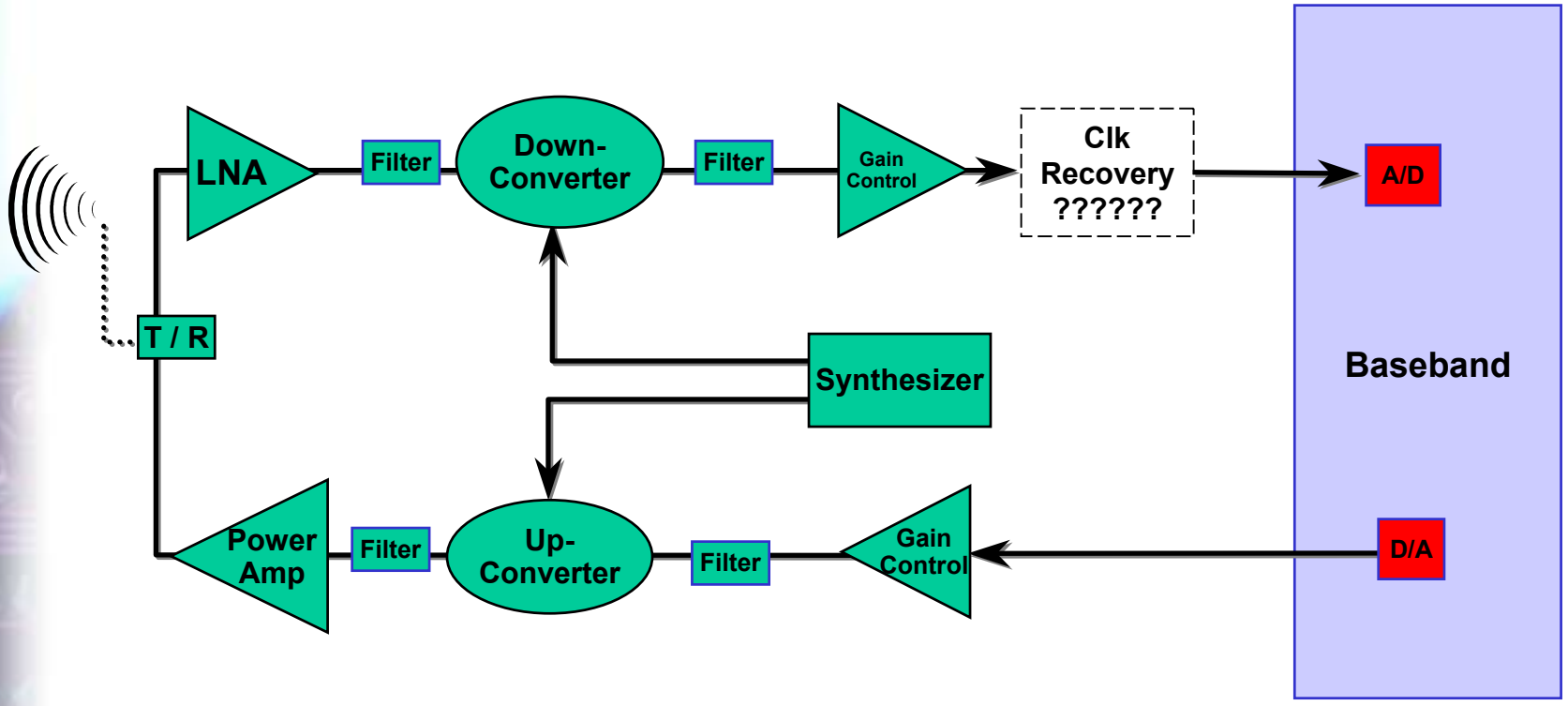
0.25 Micron CMOS Base Process

- Cost varies linearly with process complexity
- ***Less than 10% cost/complexity difference between BiCMOS and RF CMOS***

Major Factors that Drive Solution Cost and performance

- Die Size
  - Analog process means small die size for RF and easier to have better performance, lower cost??
- System Architecture and Circuit Design Implementation
  - RF-skilled companies focus on RF
    - Skill to accommodate process, temperature, voltage, and external component value variations?
    - Small external Component Count
  - Digital-skilled companies focus on digital logics
    - Digital portion integrated with functions means lower cost
    - Leverage economy of scale in volume running in digital process

Example of today RF Baseband partitioning



RF Baseband interface

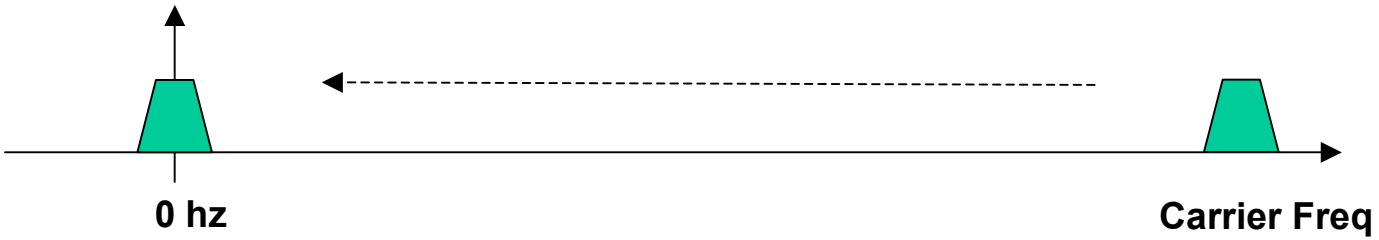
- Analog
  - Save pins
  - No noise from A/D, D/A converters
- High speed Serial interface
  - A/D, D/A in RF chips
  - Easy RF chip placement
  - Use best process for cost and performance trade off
  - Easy to support high frequency spectrum in the future
  - Difficult to define a standard

Solution to the Wireless Integration

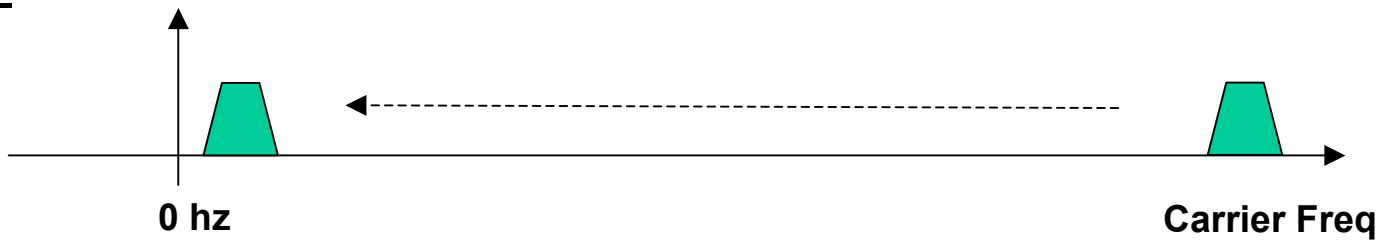
- Choose the right architecture, die cost and manufacturing yield can be optimized
  - MAC & Baseband (PHY) implemented in generic CMOS process
    - Easily integrated into infrastructure block like Southbridge
  - Radio implemented in the correct process to optimize cost and performance
    - Located away from the GHz-processor with interfering harmonics
- Need well-defined standard-based real-time digital interface between Baseband and Radio

RF Architecture

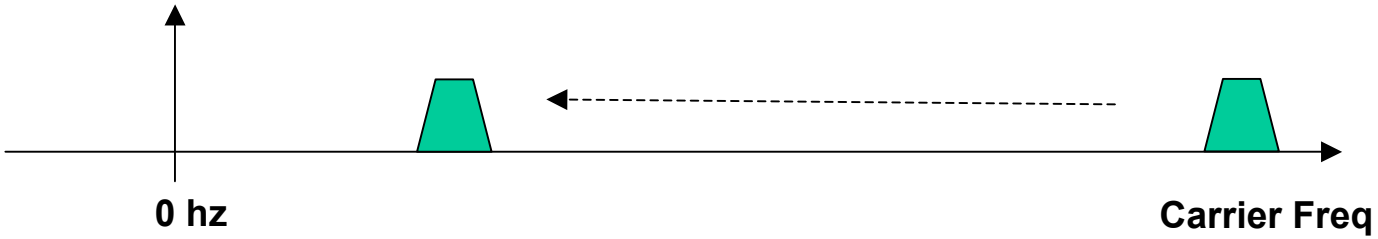
Direct Conversion



Low IF



Double Conversion



Difficulty in defining RF Baseband link

- Tight relationship between Baseband and RF architecture
  - Need to define more than just physical signals
  - Message passing between Baseband and RF
  - Still need co-operation in tuning
- Numbers of proprietary interface

Conclusion

- Serial I/O integration into Southbridge will encompass PHY in long term
- Wireless integration necessitate an industry-standard digital interface between RF & Baseband well defined and supported
  - Must be implementable by multiple vendors
- ALi is committed to provide state-of-the-art HTT Southbridges with new I/O functionalities